

PHEMT device for microwave power applications based on a double delta doped heterostructure with a stop etch layer

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In this work, we have compared the DC and RF performances of two different PHEMT devices both based on a double δ doped AlGaAs/InGaAs/AlGaAs Strained Single Quantum Well, with the gate evaporated either on an AlGaAs surface or on a GaAs one. In the last case an AlAs stop etch layer was introduced in the vertical structure. The effects on the stability of the RF performances during the device RF operation when the gate evaporation was performed either on GaAs or on AlGaAs were investigated too.

Introduction

HEMTs can be used as microwave devices (above the X band) for power applications such as satellite and urban link. Pseudomorphic HEMTs based on a double δ doped AlGaAs/InGaAs/AlGaAs Strained Single Quantum Well (SSQW) [1] are very promising for applications which need both high frequency, high power performances and low DC consumption. Silicon planar doping (δ doping) techniques are commonly used instead of step doping, in order to improve both the high frequency performances (higher g_m , higher f_T) and gate-drain diode breakdown voltage. Planar dopings are usually inserted inside each AlGaAs barrier to obtain a desired 2Dimensional Electron Gas (2DEG) inside the InGaAs channel. The high conduction band gap discontinuity between the AlGaAs alloy and the InGaAs one gives a better confinement of the 2DEG inside the channel, moreover InGaAs alloy has good electron transport properties too. On the other side, a barrier formed by an AlGaAs alloy can introduce some difficulties both during the epitaxial growth of the heterostructure and during the technological process: AlGaAs alloy is easily oxidable and Dx traps [2] can appear when AlGaAs is doped with Silicon. This last problem can be solved if a low enough Al molar fraction (x) in the AlGaAs alloy is used ($x < 0.22$) [2]. The oxidation process of the AlGaAs surface on which the gate is usually evaporated takes place during the chemical etch of the gate recess.

Both the reliability and the power and frequency performances of PHEMT devices can be reduced if a high trap concentration is present on the AlGaAs surface after the gate recess [3]. In this study, we have compared both DC and RF performances of PHEMT devices with the gate evaporated either directly on the AlGaAs barrier or on a thin GaAs layer.

In the latter case, the AlGaAs barrier was entirely covered by a GaAs layer which protected the AlGaAs surface during the etch for the gate definition. A very thin AlAs stop etch layer was introduced in the cap layer to separate the n-doped GaAs layer, needed for ohmic contact, from the thin undoped GaAs layer on which the gate was evaporated. The RF power performance degradation sometimes observed in our samples during RF operation time was attributed to the great difficulty in the control of the oxidation process on the AlGaAs surface during the gate recess.

Experimental

PHEMT structures were grown by Low Pressure Metallorganic Vapor Phase Epitaxy technique on semi-insulating GaAs (100) substrates 2° off misoriented toward the $\langle 110 \rangle$ direction. Details on growth conditions have been described elsewhere [4].

The vertical structure for the heterostructure without the stop etch layer (type A) was formed by a 400 nm undoped GaAs / 100 nm $\text{Al}_{0.22}\text{GaAs}$ buffer layer, a $\text{Si } \delta_2$ doping of about $1.3 \times 10^{12} \text{ cm}^{-2}$, a 3 nm undoped $\text{Al}_{0.22}\text{GaAs}$ spacer, a 14.5 nm undoped $\text{In}_{0.18}\text{GaAs}$ channel, a 3 nm undoped $\text{Al}_{0.22}\text{GaAs}$ spacer, a $\text{Si } \delta_1$ doping of about $1.5 \times 10^{12} \text{ cm}^{-2}$, a 30 nm undoped $\text{Al}_{0.22}\text{GaAs}$ Schottky layer, a 10 nm undoped GaAs spacer followed by a 40 nm Si doped ($5 \times 10^{18} \text{ cm}^{-3}$) GaAs cap layer.

The heterostructure with the stop etch layer (type B) was different from the previous structure because the Schottky layer was formed by a 25 nm undoped $\text{Al}_{0.22}\text{GaAs}$ layer covered by a 5 nm undoped GaAs layer followed by 2 nm Si doped ($1.5 \times 10^{17} \text{ cm}^{-3}$) AlAs stop etch layer and a 50 nm Si doped ($5 \times 10^{18} \text{ cm}^{-3}$) GaAs cap layer. The AlAs was n-doped with Silicon in order to prevent the unintentional p-type doping which takes place when the AlAs is MOVPE grown [2].

The GaAs cap layer, needed for ohmic contact, was removed during the gate recess by a wet selective etch based on $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ solution. The Ti/Pd/Au gate was then evaporated directly on the AlGaAs Schottky layer if the type A heterostructure was used. In this case, a strong oxidation of the AlGaAs surface took place when the selective etch, used for the gate recess, stopped at the GaAs/AlGaAs interface. The $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ solution is used for a time longer than the one needed to remove the 50 nm GaAs cap layer. This overetching time was introduced to increase the width of the gate recess in order to increase the gate-drain diode breakdown voltage.

The AlAs stop etch layer inserted inside the type B vertical structure allowed us to remove the GaAs cap layer using the same etching solution. In this case, the selective etch completely stopped at the GaAs/AlAs interface due to the very high selectivity ratio between the etching rates of GaAs and of AlAs. On the contrary, when the GaAs / $\text{Al}_{0.22}\text{GaAs}$ interface was used to stop the etch during the gate recess, the etching rate didn't fall to the same very low value as in the case of the GaAs / AlAs interface. The AlAs layer was later removed by a second selective etch with an HF based solution, which stopped selectively at the AlAs/GaAs interface. Moreover, the HF solution was also a desox etch for the GaAs surface. Therefore using the AlAs stop etch layer the gate was evaporated on a GaAs surface cleaned with a desox solution. Even if an oxidation process took place on the GaAs surface, its magnitude is certainly reduced with respect to that on the AlGaAs surface wetted by $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ solution.

Results and discussion

Fig.1a and Fig.1b show the conduction band and the valence band calculated for type A and type B heterostructures respectively. The calculation was performed by solving the Schrödinger equation and the Poisson equation in a self-consistent way using the same built-in potential.

The I-V curves obtained measuring devices with and without the stop etch layer are shown in fig. 2a and fig. 2b respectively. Table 1 and table 2 show for each kind of heterostructure, the DC performances and the RF ones. Some variation in the DC performances of PHEMTs with or without the stop etch layer was observed probably due to a little difference in the values of built-in potentials between a Schottky diode realized on AlGaAs and on GaAs; this can give a little change in the 2DEG inside the channel, even if the nominal δ doping is the same. On the contrary, the gate-drain diode

ideality factor was 1.3 and it didn't change if the gate was evaporated either on GaAs or on $\text{Al}_{0.22}\text{GaAs}$. The high selectivity ratio of the $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ etching solution used to remove the GaAs cap layer, allowed us to keep the thickness of the AlAs stop etch layer at a very low value (2 nm). The thin AlAs layer under the ohmic contact, which wasn't removed during the gate recess, didn't produce any change on the access resistances as can be showed by comparing the slope of the I-V curve in the linear regime (fig.2a and 2b). We observed a strong reduction of the slope of the I-V plot in the linear region only when relatively thick (10-20nm) AlAs stop etch layers were used, even if the electrons injected through the ohmic contact shouldn't meet any barrier moving across the AlAs layer because the conduction band gap discontinuity between AlAs and GaAs is very small due to the indirect band gap of the AlAs [2]. This could be explained if a thick enough AlAs layer could stop the diffusion of the GeNiAu alloy during the ohmic contact annealing cycle. The RF performances obtained for devices based on type A and type B heterostructures are about the same (table 2) at time = 0.

In some samples we observed a degradation of the power at 1dB gain compression. In fig.3 we have reported the power degradation behaviour during RF time operation observed for two set of 10 devices based on type A or type B heterostructure which showed the power degradation. We attributed the observed power degradation to the formation or activation of traps in the gate-drain access region during the RF device operation [3;5]; if these traps change their ionization state during the RF operation, a change of the surface potential under the gate-drain access region took place and a quenching of the electron density inside the channel could happen. If these traps were formed on the surface due to the oxidation process during the gate recess, then the higher oxidation of the AlGaAs respect to the GaAs could explain the higher RF degradation observed in PHEMT devices based on type A heterostructure, where the gate was directly evaporated on the AlGaAs alloy.

Table 1: DC performance

	Current density @ $V_{gs}=0V$ $V_{ds}=3V$ (mA/mm)	Gate-drain diode breakdown voltage (V)	Max transconductance @ $V_{ds}=3V$ (mS/mm)
type A	323	-8.4	265
type B	389	-5.1	260

Table 2: RF performance

	RF Power @ 1dB gain compression (dBm)	Gain (dB)	Efficiency (%)
type A*	21.5	10.4	38.3
type B**	21.2	10.3	29
type A°	20.1	6.58	23

* : $f = 7.5$ GHz, $V_{ds}=5V$, $I_{ds}=90mA$, gate width= 260 μm , gate length=0.5 μm

** : $f = 7.5$ GHz, $V_{ds}=5V$, $I_{ds}=110mA$, gate width= 260 μm , gate length=0.5 μm

° : $f = 18$ GHz, $V_{ds}=5V$, $I_{ds}=90mA$, gate width= 260 μm , gate length=0.5 μm

References

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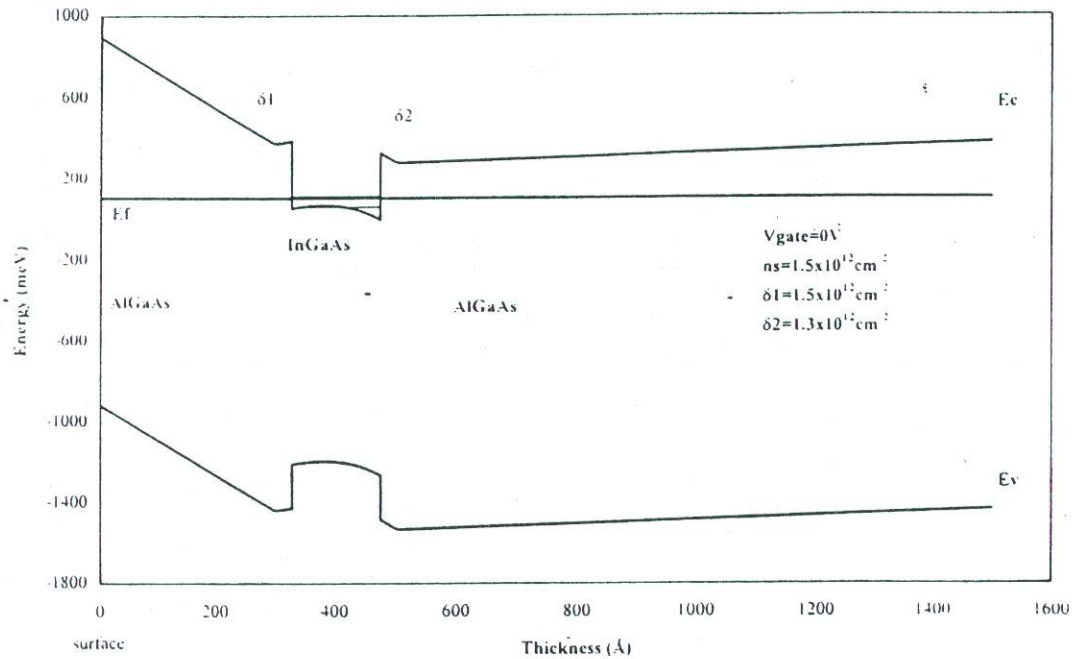


Fig.1a - Band diagram , type A

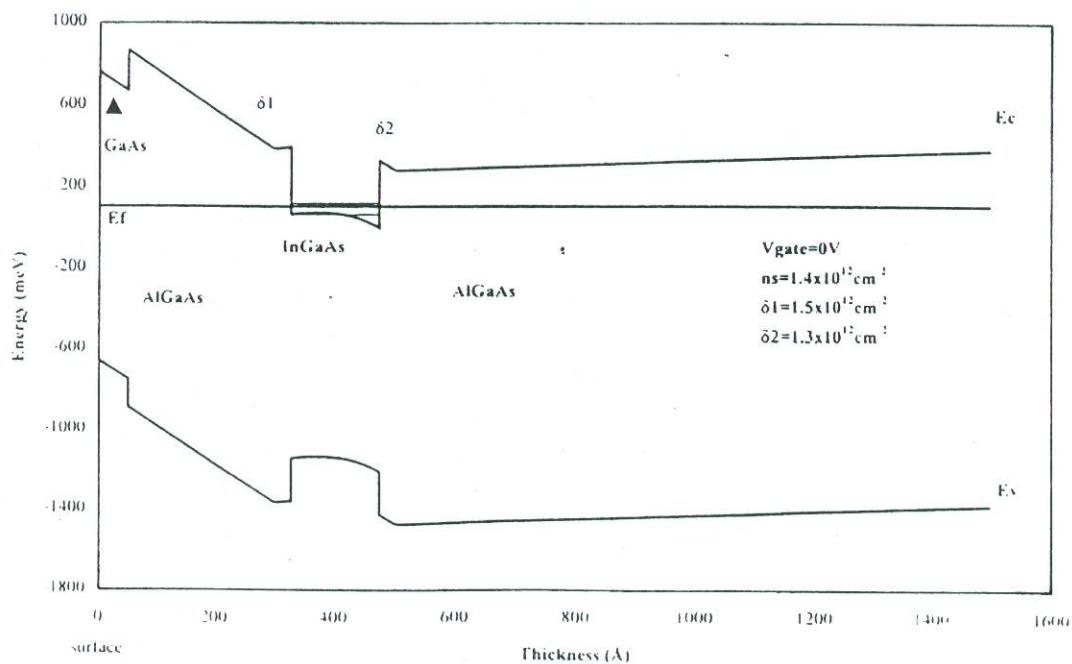
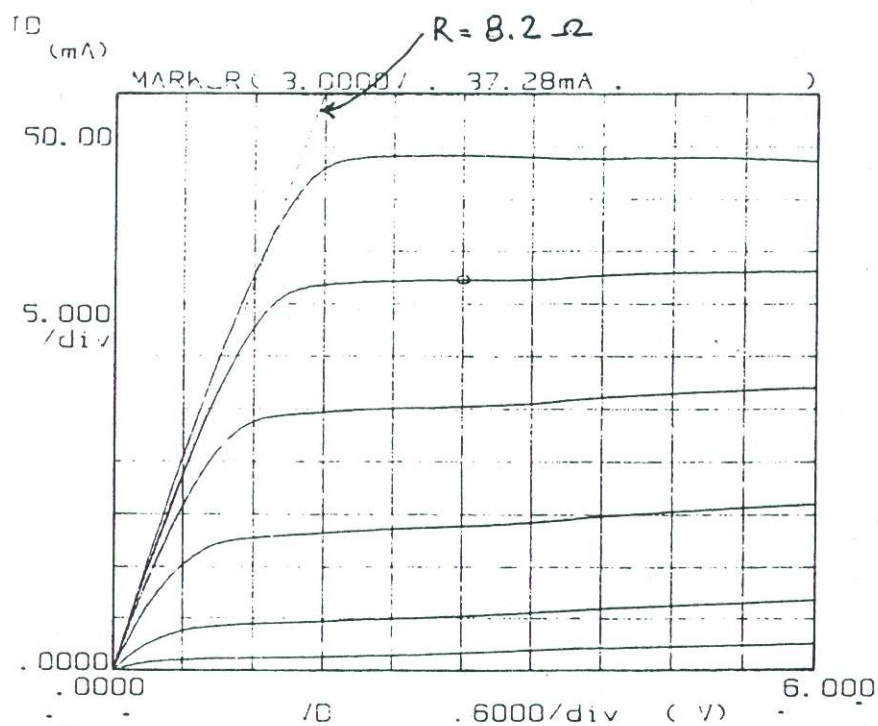


Fig.1b - Band diagram , type B



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Variable1:
/D Ch1
Linear sweep
Start .0000/
Stop 6.0000/
Step .1000/

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Variable2:
/V Ch2
Start .5000/
Stop 2.5000V
Step .5000/

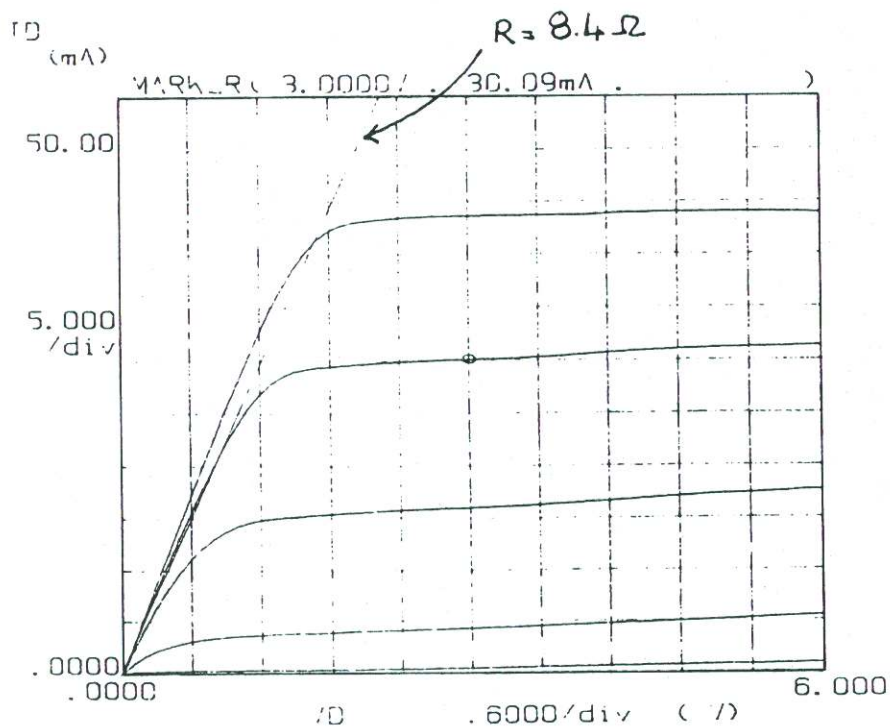
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```

Constants:
/ Ch3 .0000V

```

Fig.2a - I-V curves , type A



```

Variable1:
/D Ch1
Linear sweep
Start .0000/
Stop 6.0000/
Step .1000/

```

```

Variable2:
/V Ch2
Start .5000/
Stop 1.9990V
Step .5000/

```

```

Constants:
/ Ch3 .0000/

```

Fig.2b - I-V curves , type B

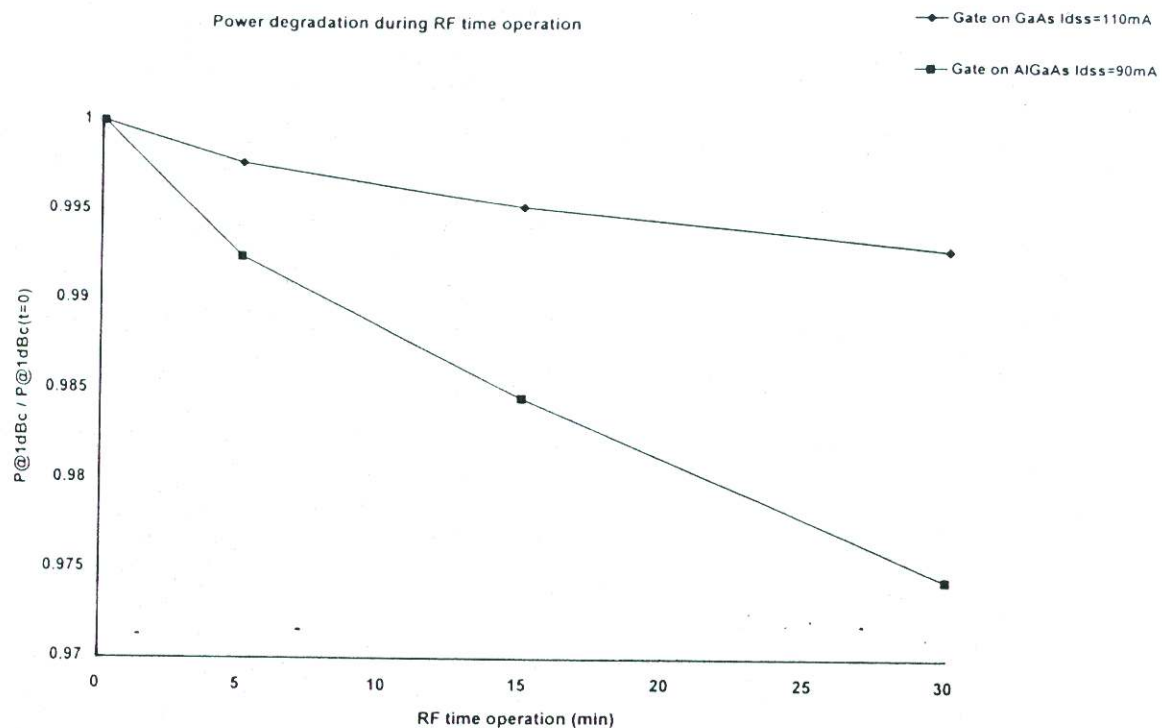


Fig.3 - Power degradation , type A and B devices